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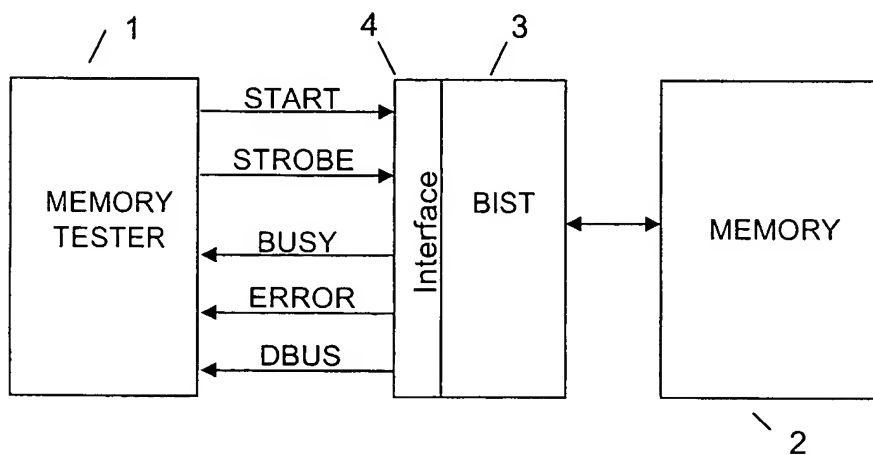


FIG. 1a

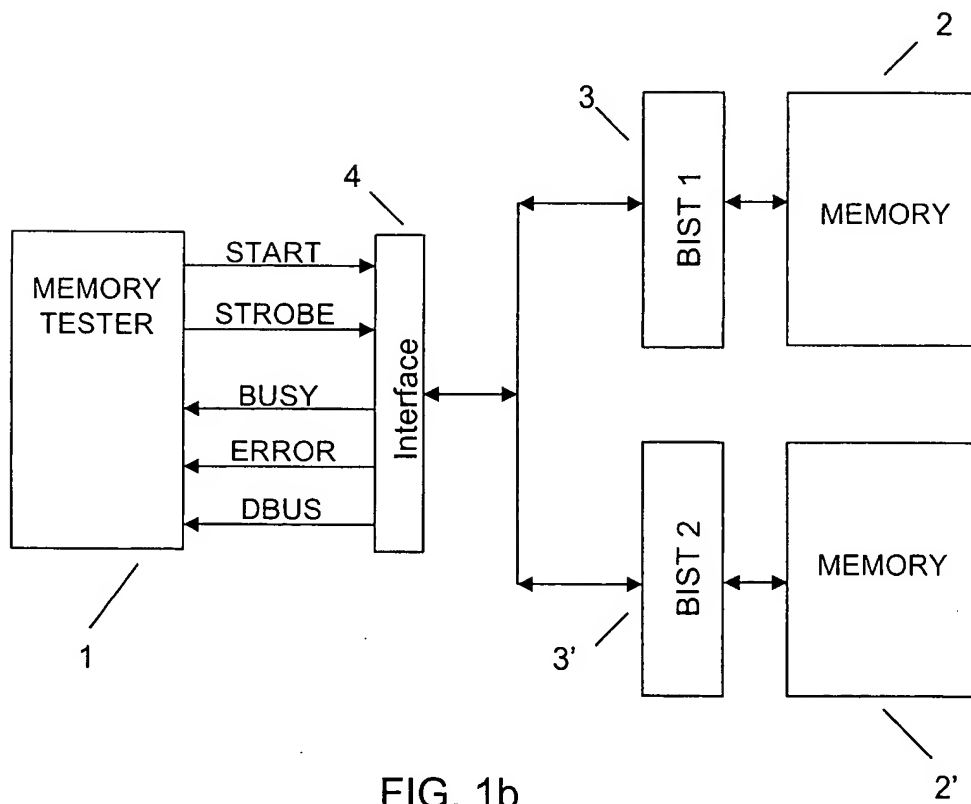


FIG. 1b

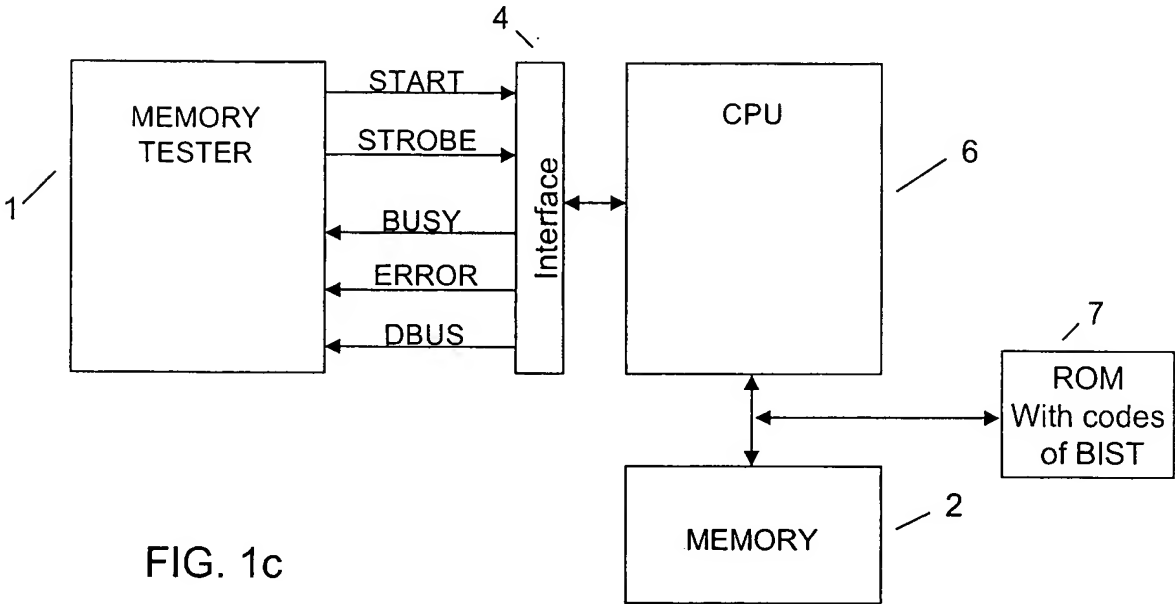


FIG. 1c

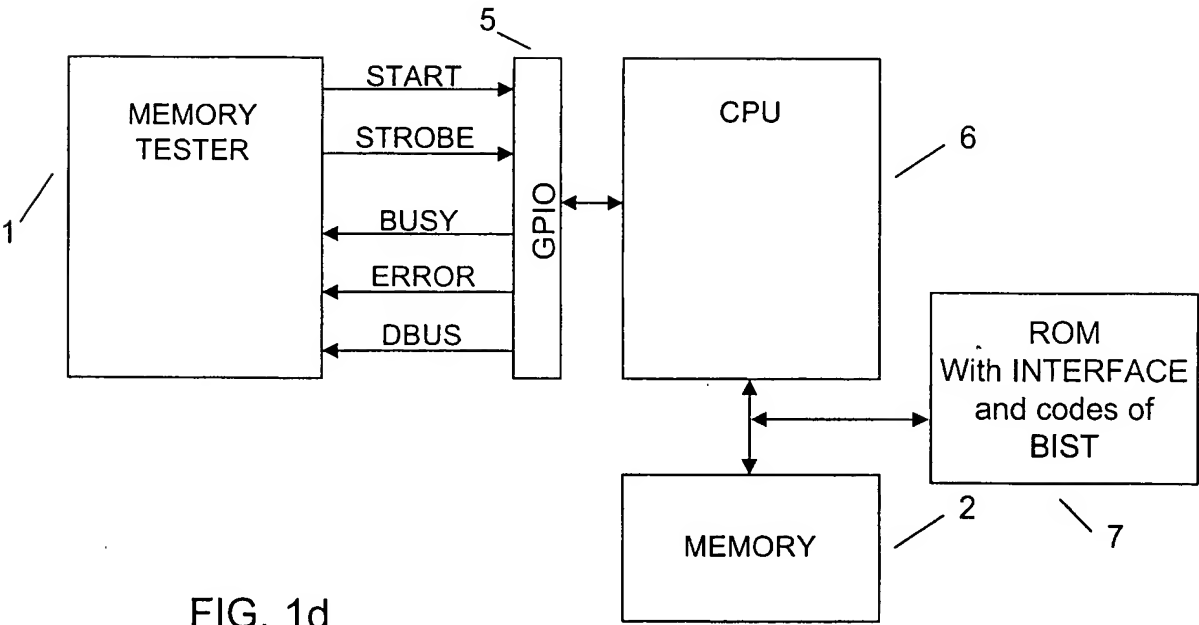


FIG. 1d

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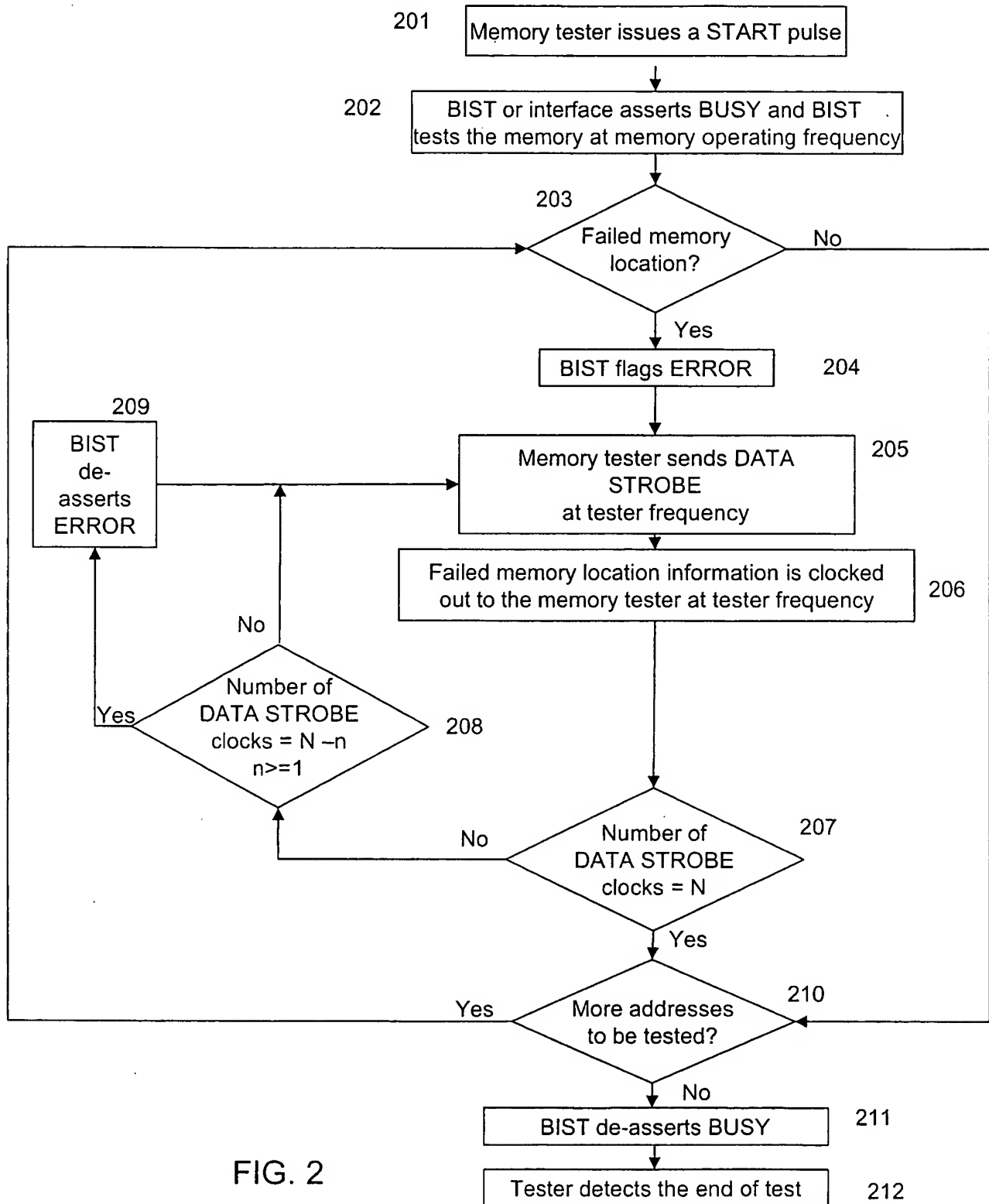


FIG. 2

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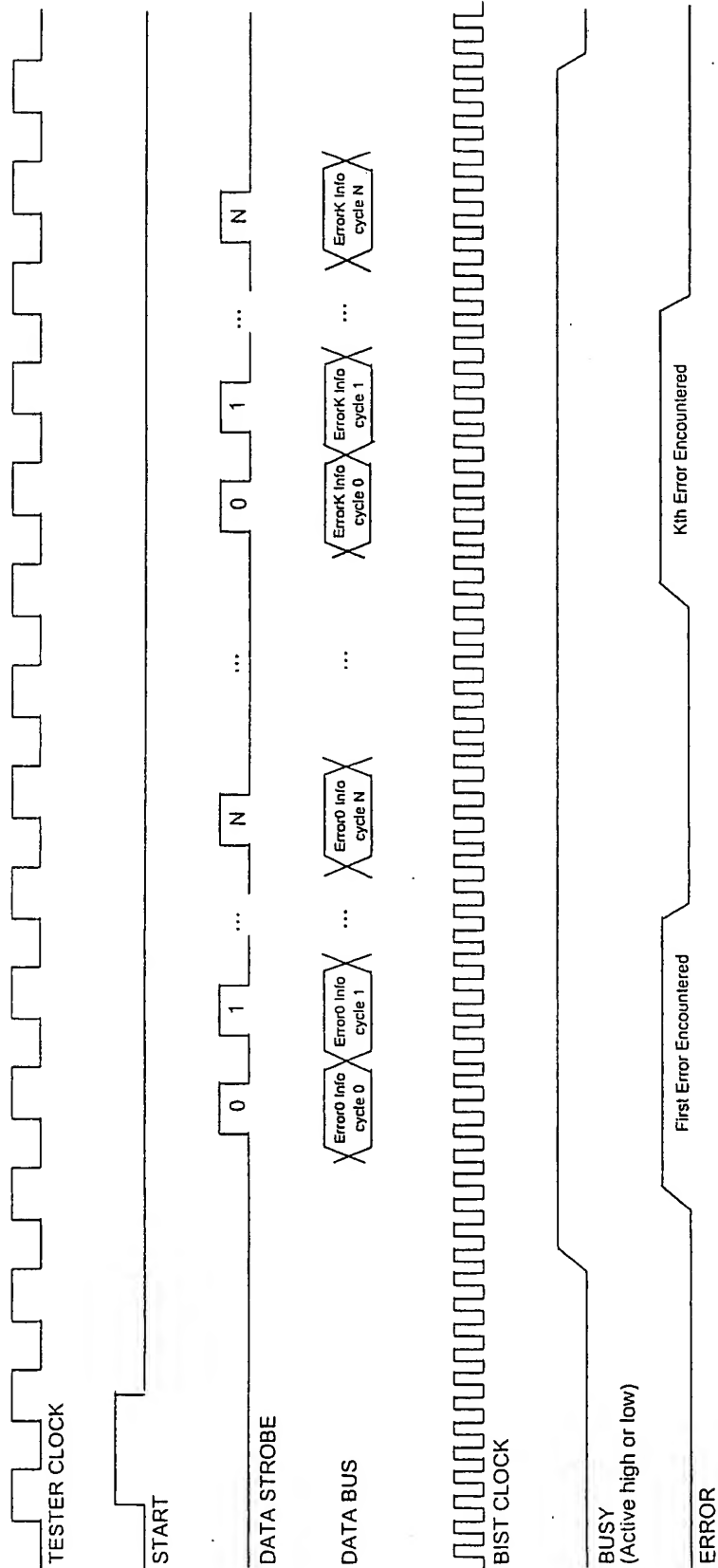


Fig. 3

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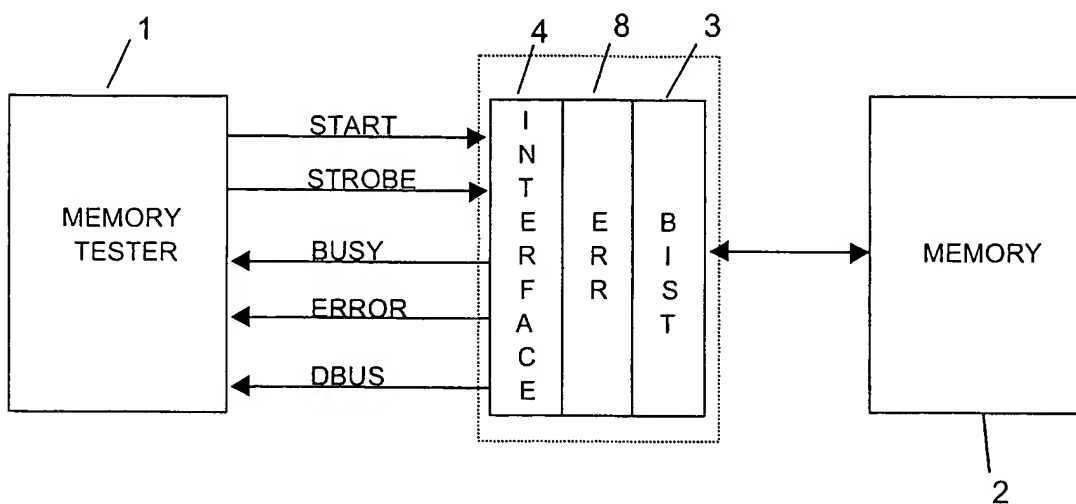


FIG. 4a

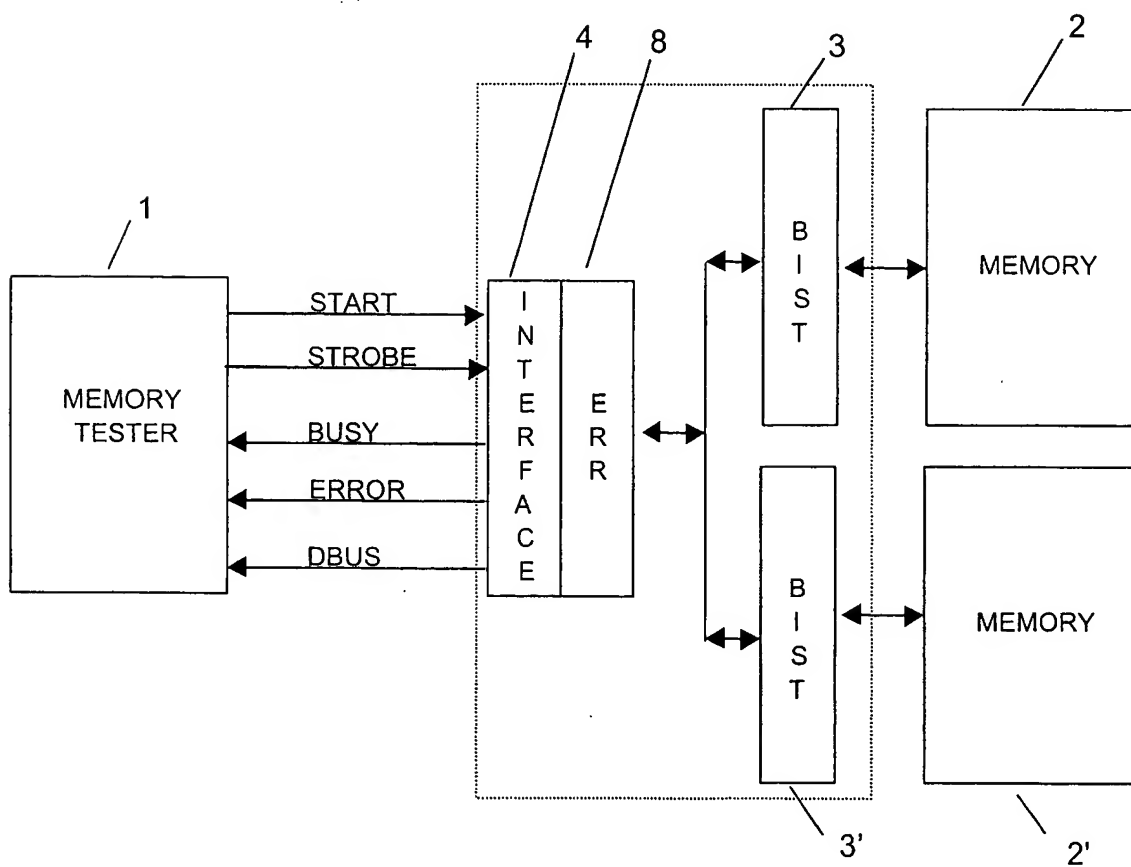


FIG. 4b

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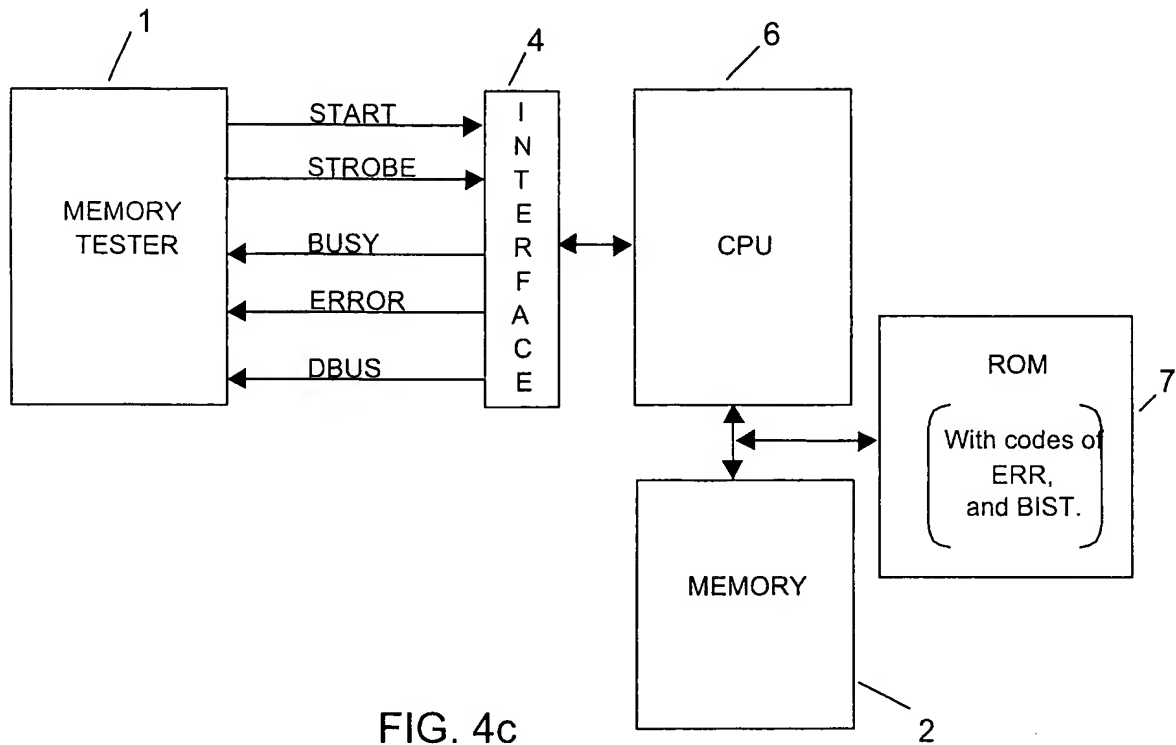


FIG. 4c

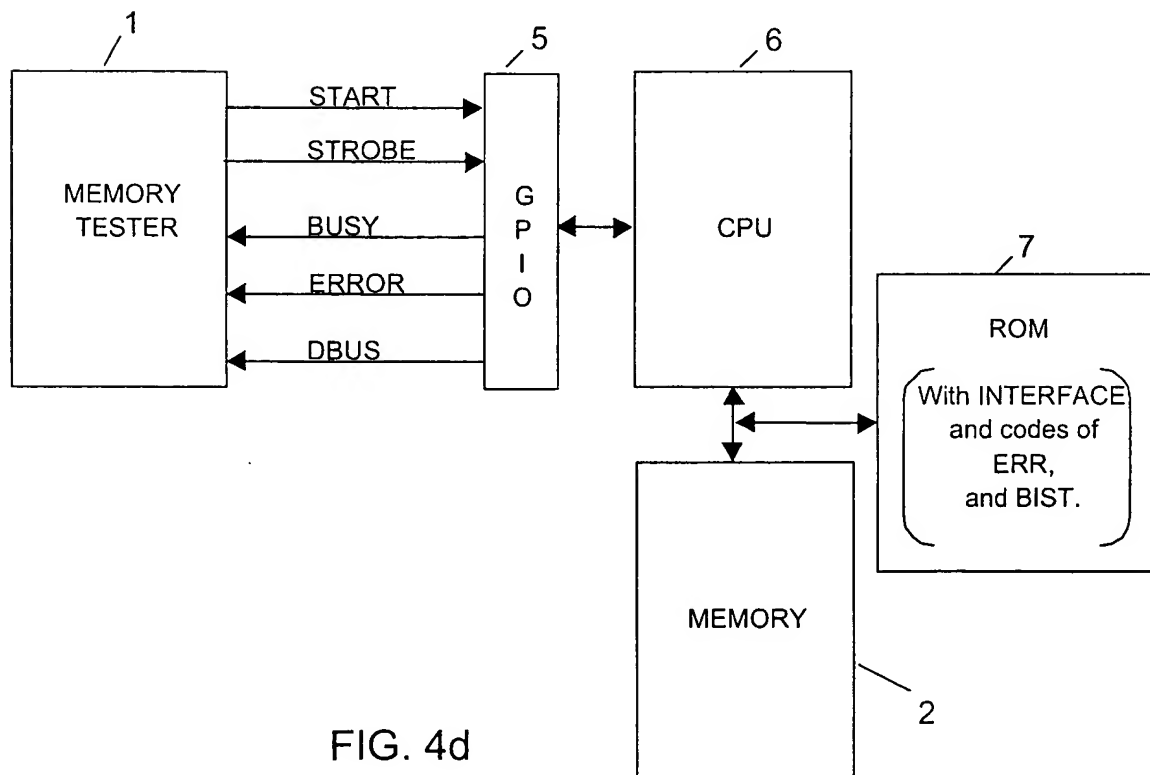


FIG. 4d

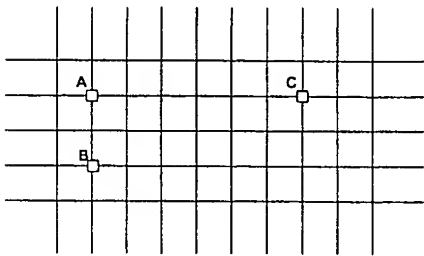


Fig. 5a

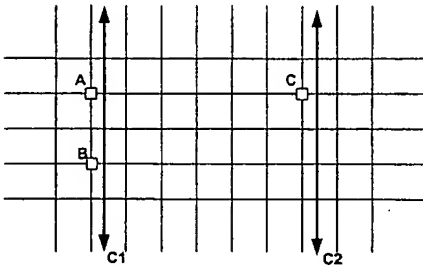


Fig. 5b

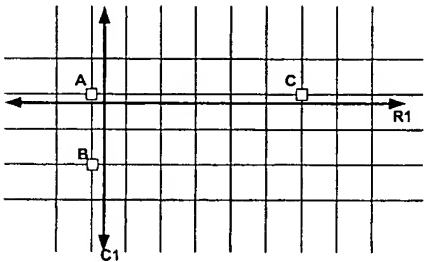


Fig. 5c

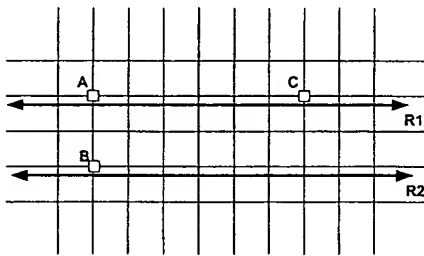


Fig. 5d

	ROW	COLUMN	BIT POSITION	EV	RG1	RGTX	CG1	CGTX	RF	CF
0	Row Addr A	Col Addr A	(A) I/O error Positions	1	1	0	1	0		
⋮										
N										

BAD LIST
(BL)

Fig. 5e

	ROW	COLUMN	BIT POSITION	EV2	RF2	CF2
←	Row Addr B	Col Addr C	(C) I/O error Positions	1		
←						
←						
←						

ASSOCIATED BAD LIST
(ABL)

Fig. 5f

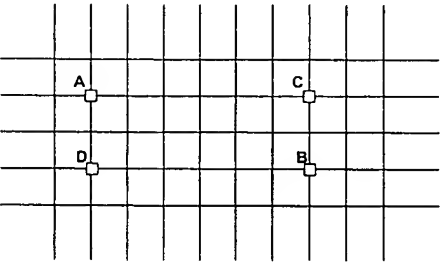


Fig. 6a

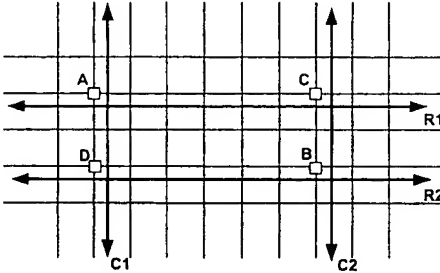


Fig. 6b

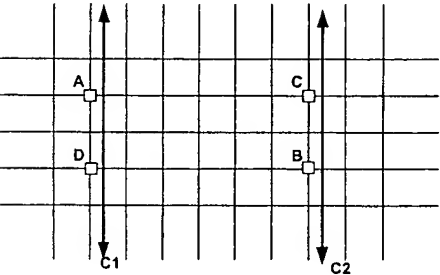


Fig. 6c

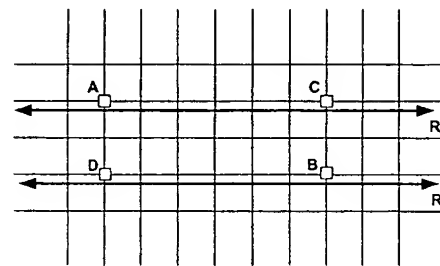


Fig. 6d

	ROW	COLUMN	BIT POSITION	EV	RGT1	RGTX	CGT1	CGTX	RF	CF
0	Row Addr A	Col Addr A	(A) I/O error Positions	1	1	0	1	0		
⋮	Row Addr B	Col Addr B	(B) I/O error Positions	1	1	0	1	0		
⋮				0						
N				0						

BAD LIST
(BL)

Fig. 6e

	ROW	COLUMN	BIT POSITION	EV2	RF2	CF2
←	Row Addr D	Col Addr C	(C) I/O error Positions	1		
←	Row Addr C	Col Addr D	(D) I/O error Positions	1		
←				0		
←				0		

ASSOCIATED BAD LIST
(ABL)

Row Addr B = Row Addr D
Col Addr B = Col Addr C

Fig. 6f

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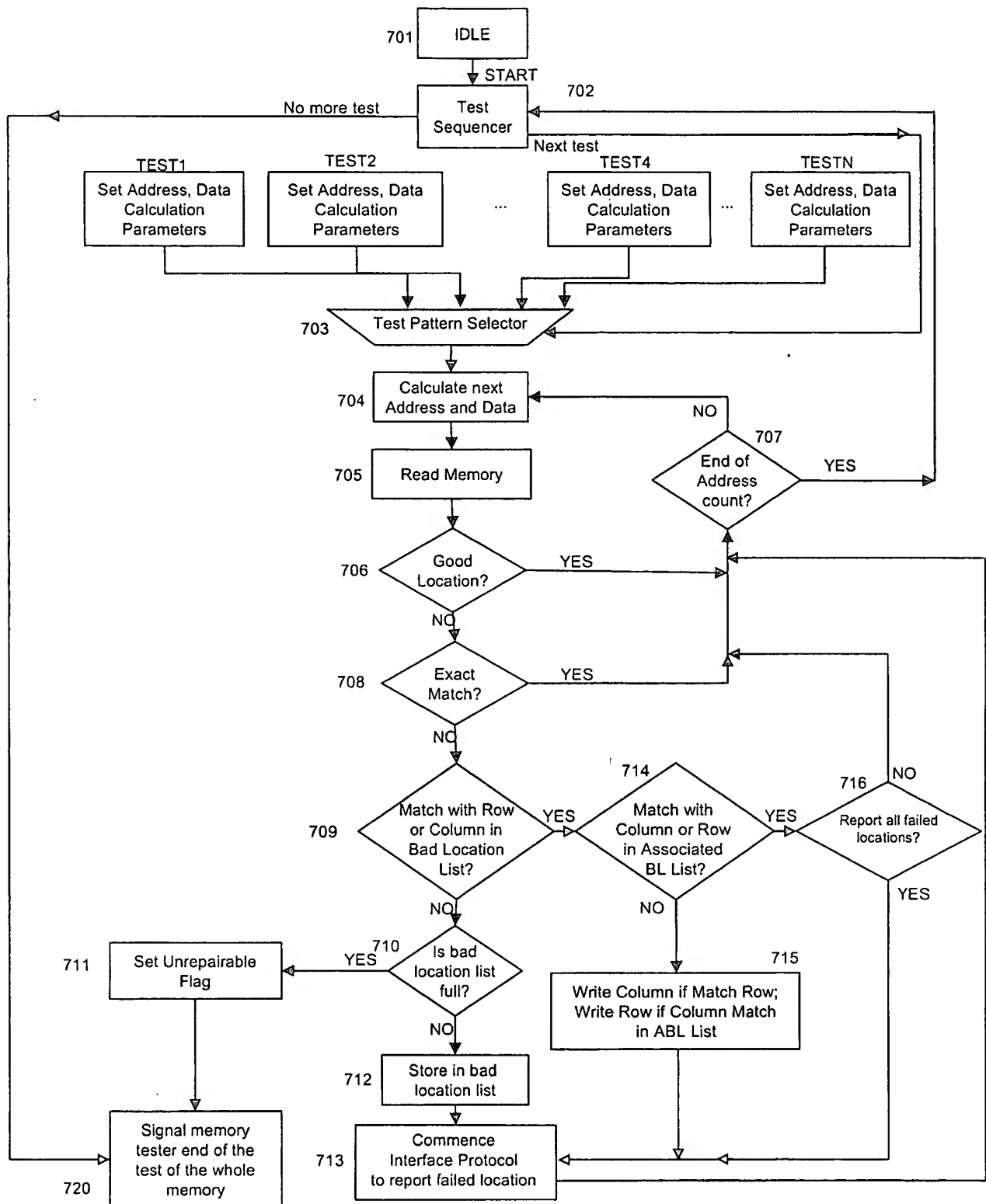


FIG. 7

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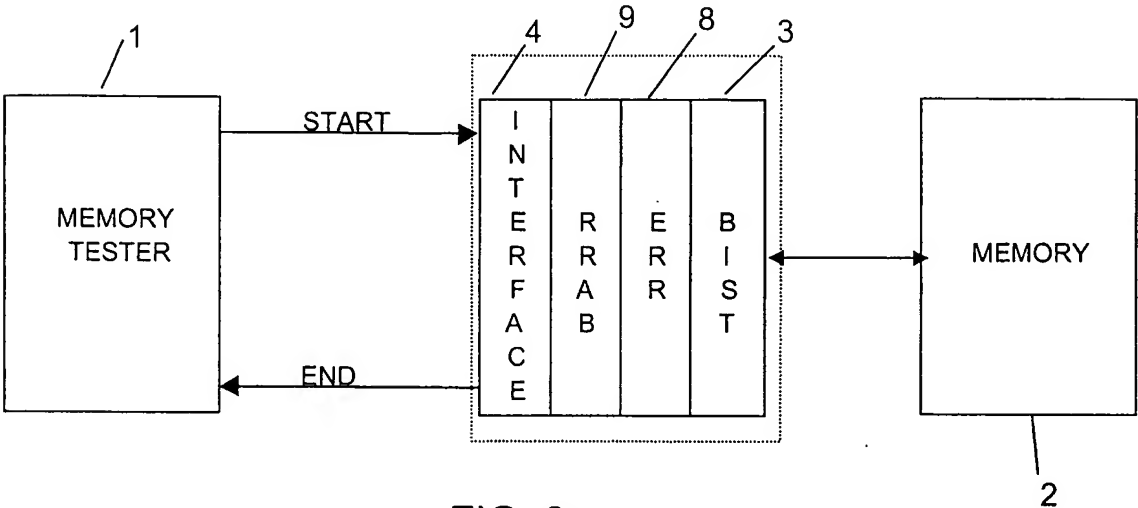


FIG. 8a

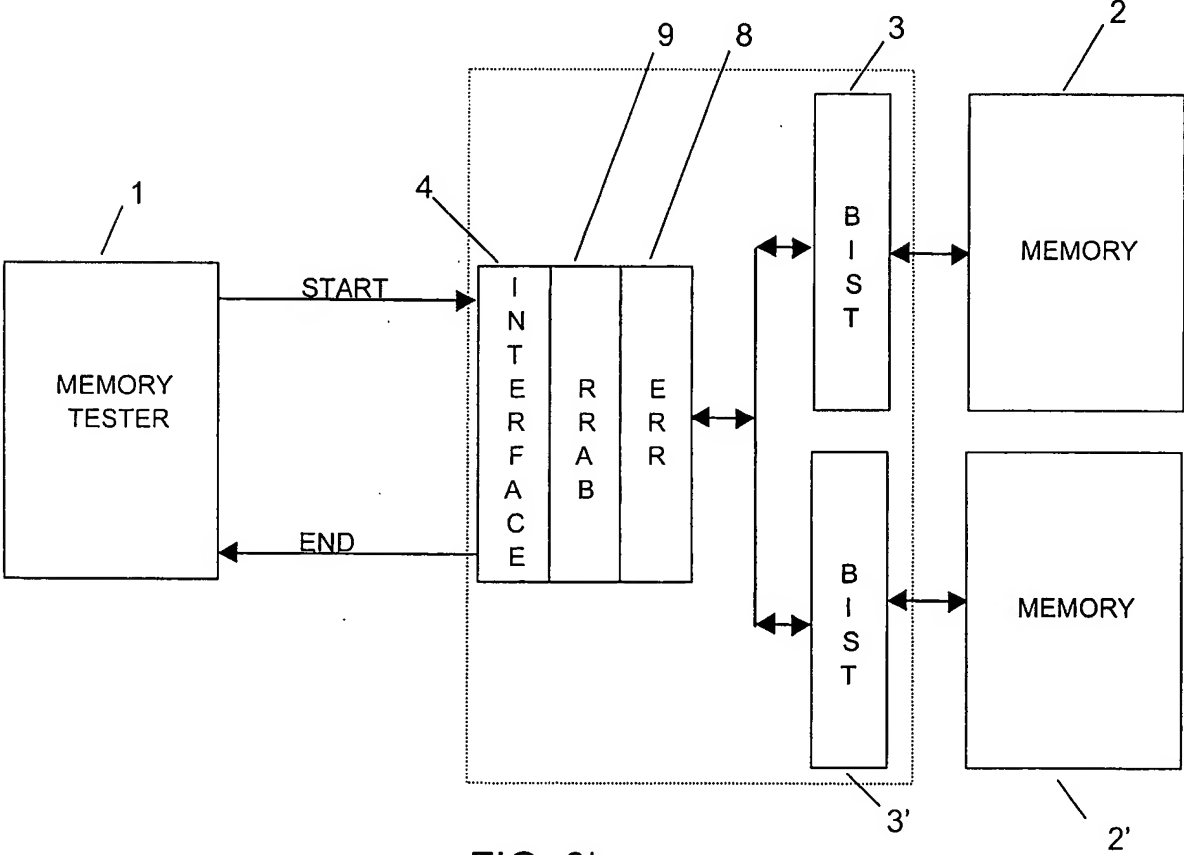


FIG. 8b

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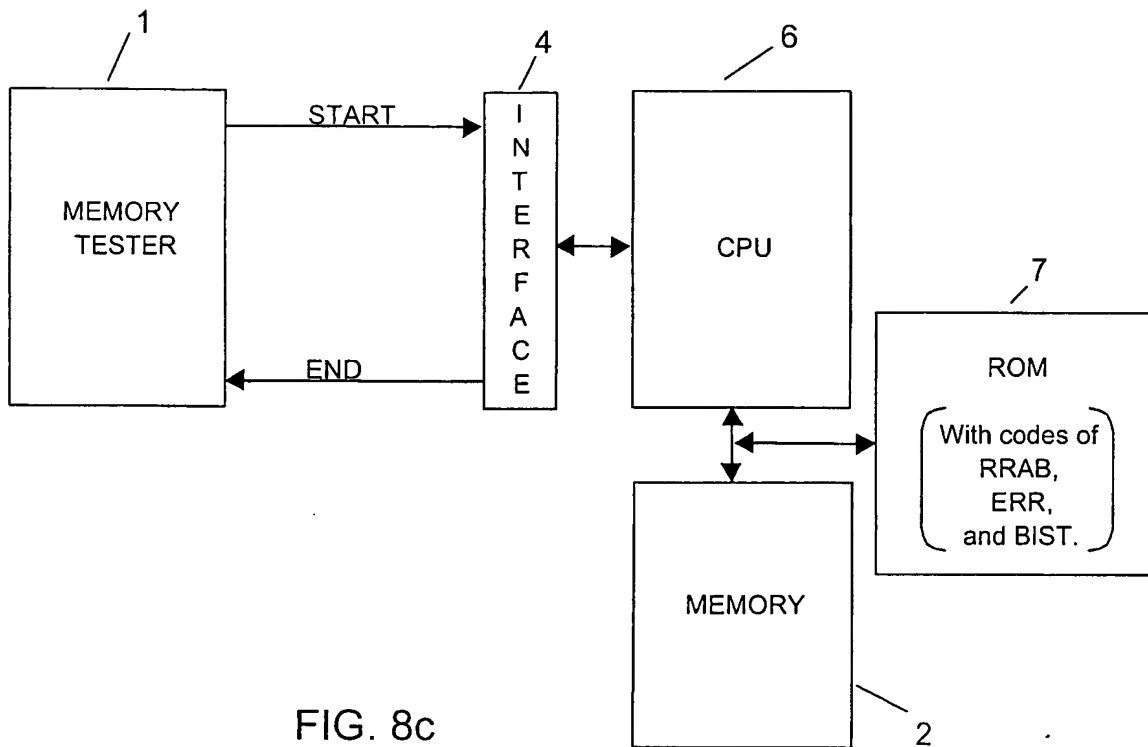


FIG. 8c

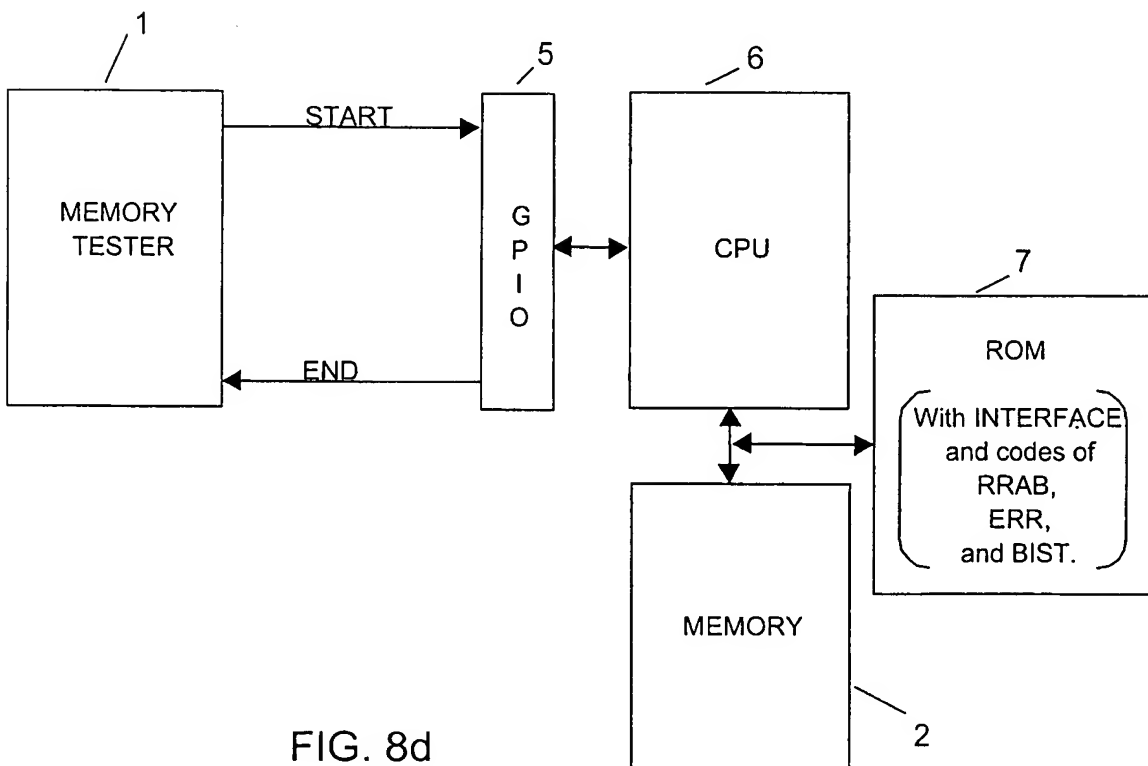


FIG. 8d

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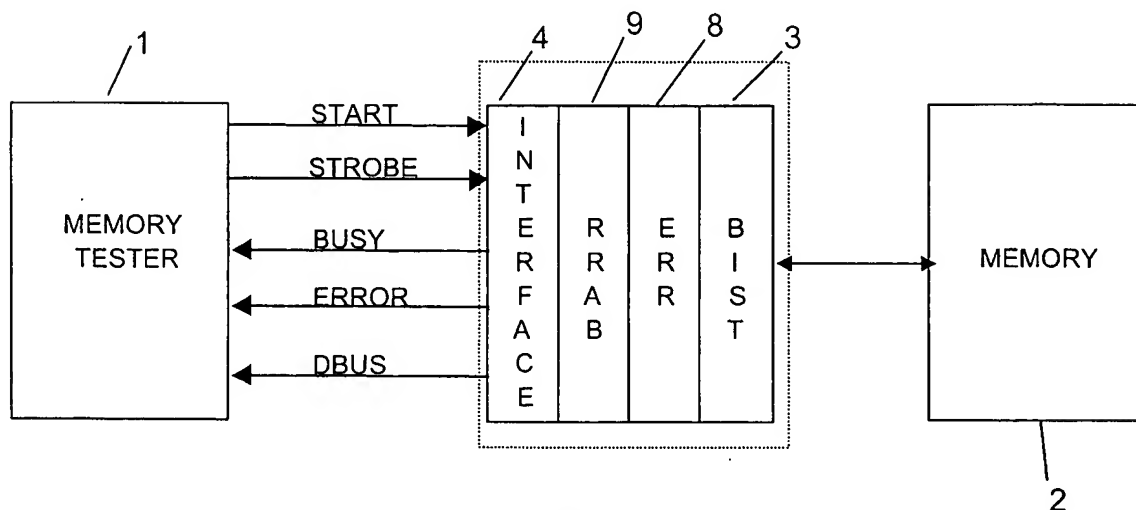


FIG. 8e

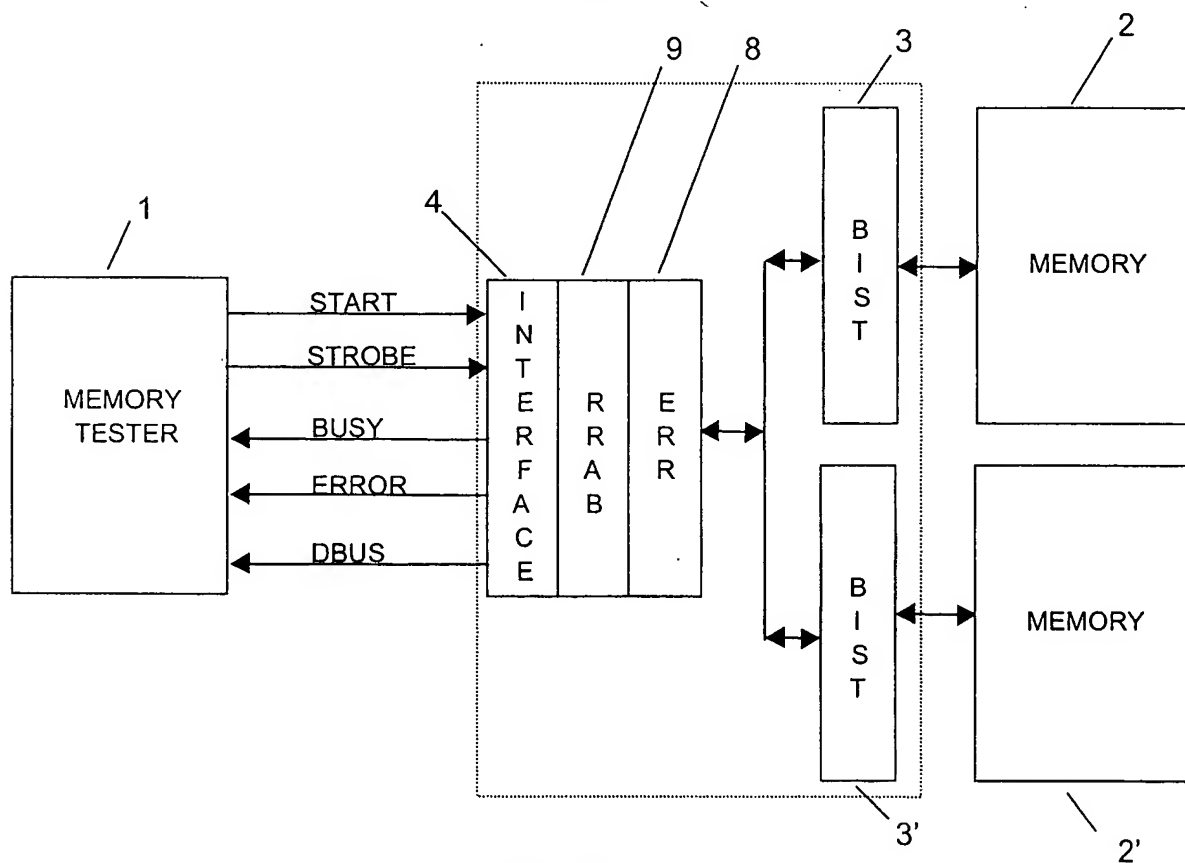


FIG. 8f

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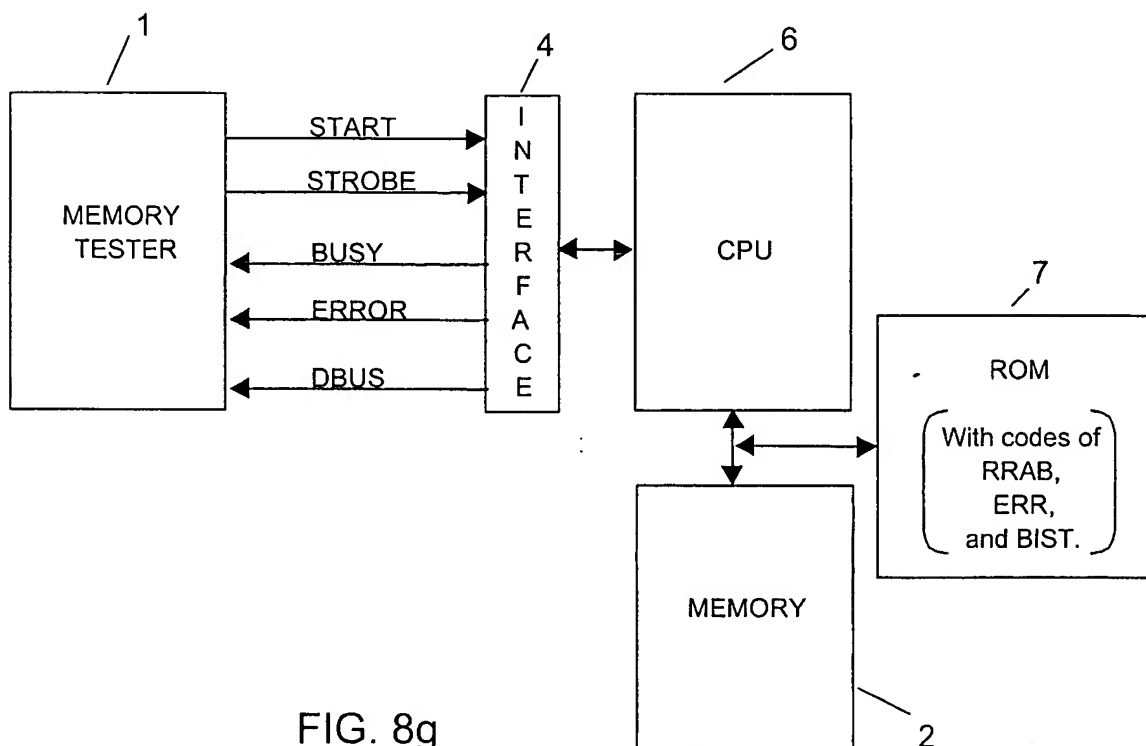


FIG. 8g

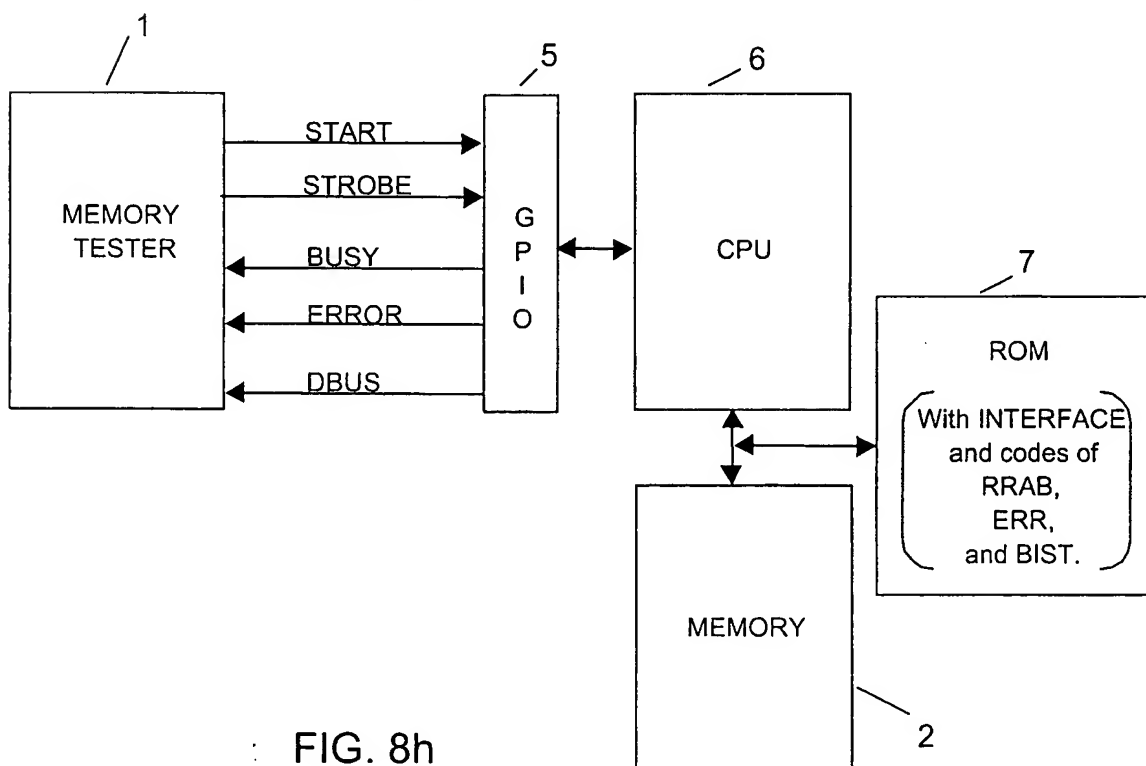


FIG. 8h

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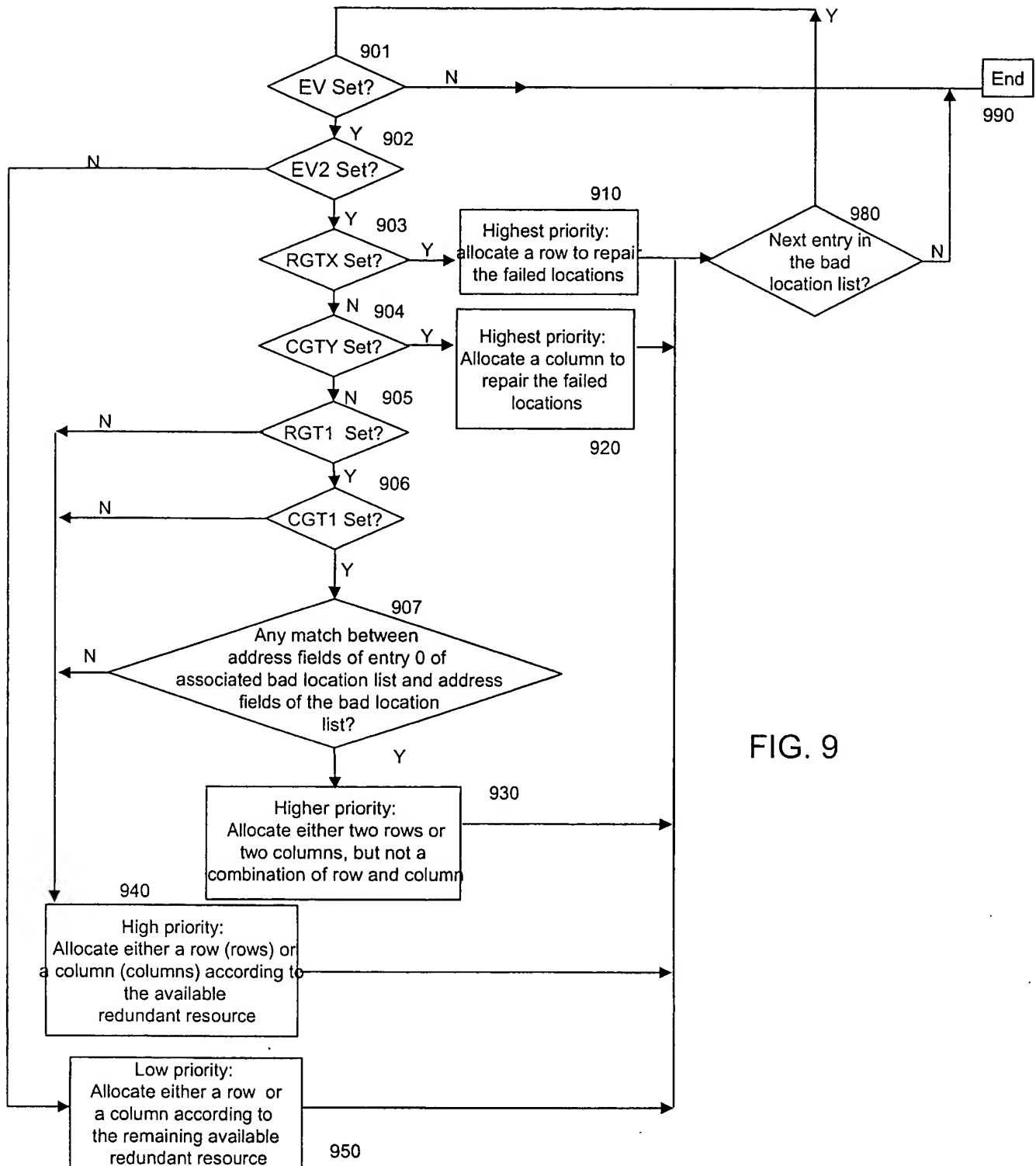


FIG. 9